REMARKS

In the Office Action mailed January 26, 2007, claims 1-8, 10-13 and 15-30 are rejected under 35 USC §103(a) as being unpatentable over Levi et al. (U.S. Patent 6,363,517, "Levi") in view of Miller et al. (U.S. Pub. No. 20020121913, "Miller"). Applicants have amended the claims in view of the Examiner's comments, and believe that the claims as amended are in a condition for allowance.

Before addressing new amendments, Applicants would like to respond to the assertion that Levi discloses a plurality of devices having different programmable logic device architectures. Applicants respectfully submit the Levi expressly teaches away from using a plurality of FPGAs having different programmable logic device architectures. It is suggested in the Office Action that the description of Fig. 8 in Col. 13, lines 15-29 of Levi discloses systems under test having different programmable logic device architectures. However, while three FPGAs are described in Col. 13, lines 15-29, there is simply no teaching or even a suggestion that these FPGAs could have different programmable logic device architectures. In contrast, Levi expressly teaches that, when an FPGA design is being evolved on several FPGAs in parallel, the various FPGAs have common architectures so they will respond the same way to the same subset of a bitstream. (Col. 11, lines 46-50). For example, evolving bitstreams for the design of a counter in an FPGA1 and an FPGA2 would require an FPGA having the same architecture according to the Levi. Assuming that the counter and the controller are implemented as a part of the same design, the FPGA1, FPGA2 and FPGA3 would have to the same architecture.

However, to avoid any ambiguity, Applicants have amended each of the independent claims to indicate that the design coupled to a device under test is the design to be tested. Applicants have further amended each of the independent claim to expressly claim that each of the systems under test having different programmable logic device architectures is coupled to receive the design of a programmable logic circuit to be tested. That is, each system under test receives configuration data for the given design of a programmable logic circuit.

In response to the newly cited Miller reference, Applicants have also amended the claims to more clearly indicate that a server is coupled to the plurality of client

computers and the plurality of systems under test such that the plurality of systems under test receive data from or provide data to the plurality of client computers by way of the server. It is suggested in the Office Action that a plurality of client computers is disclosed by a "site host" of Miller which collects test data from individual "cell hosts." However, there is no indication that the site host in anything other than a single computer. Further, the functionality of the site host is to collect test data from individual cell hosts, and place compressed data in a central server. (Paragraph [0034]). Miller is directed to a "burn-in" tester applying various operating parameters, such as voltages or frequencies, in order to accelerate potential failures. In order to more clearly distinguish Applicants' claims over the combination of references, Applicants have amended each of the independent claims having a plurality of client computers to more clearly indicate that the system under test receives a test job from a client computer by way of the server. In contrast, Miller teaches that a cell host is coupled to the devices under test by way of a network connection, such as an Ethernet connection 201 as shown in Fig. 2. Because the system of Miller is used for burn-in testing, there is no need for a server between the plurality of cell hosts and the devices under test. Accordingly, Applicants respectfully submit that the claims as amended clearly distinguish over the combination of Levi and Miller. Applicants now refer to the specific language of each independent claim which distinguishes the claim over the combination of references.

Claim 1

Independent claim 1, which is directed to a client-server verification system, has been amended to indicate that a test job has configuration data for "the design of a programmable logic circuit," and that "each system under test of the plurality of systems under test has a programmable logic circuit and is configured with said design of a programmable logic circuit implemented according to said configuration data." Finally, Applicants have amended independent claim 1 to indicate that each system under test receives corresponding test vectors and outputs result vectors to the client computer by way of the server. Applicants respectfully submit that neither reference discloses or suggests a plurality of systems under test, where each system

under test has different programmable logic device architectures as claimed, or that each system under test is configured with a given design of a programmable logic circuit. Applicants submit that independent claim 1 as amended, and its dependent claims 2-5, clearly distinguish over the combination of references, and respectfully request reconsideration of the rejection of the claims.

Claim 6

Independent claim 6 is also directed to a client-server verification system, but comprises a plurality of client computers and a server. Applicants have also amended independent claim 6 to more clearly indicate that the configuration data comprises configuration data for the design to be tested. Applicants have further amended independent claim 6 to indicate that each system under test of the plurality of systems under test has a programmable logic circuit which is configured with the design of the programmable logic circuit implemented according to configuration data of the test job received from the client computer by way of the server, and receives corresponding test vectors of the test job. In contrast, Miller, which is cited for disclosing a plurality of client computers, fails to disclose or suggest a plurality of client computers where the plurality of systems under test receive the design of the programmable logic circuit to be tested from a client computer by way of a server. Further, neither Levi nor Miller discloses or even suggests configuring each system under test of the plurality of systems under test with the design of the programmable logic circuit to be tested.

Applicants submit that independent claim 6 as amended, and its dependent claims 7, 8 and 10, clearly distinguish over the combination of references, and respectfully request reconsideration of the claims.

Claim 16

Independent Claim 16 is directed to a method of verifying a semiconductor design by way of a server. Applicants have amended claim 16 to more clearly indicate that the configuration data comprises configuration data for the design to be tested. Applicants have further amended independent claim 16 to indicate that each

system under test of the plurality of systems under test is configured with the design of the programmable logic circuit according to configuration data of a test job received from a client computer by way of the test server. Applicants have further amended claim 16 to indicate that corresponding test vectors are coupled from the client computer to each system under test by way of the test server. Finally, Applicants have amended claim 16 to indicate that an output is received from and result vectors are compared for each system under test. For the same reasons set forth above with respect to claim 6 as amended, neither Levi nor Miller discloses or suggests configuring each system under test of the plurality of systems under test with the design of the programmable logic circuit, or coupling test vectors from the client computer to each system under test by way of the test server. Applicants submit that independent claim 16 as amended, and its dependent claims 17-20, also clearly distinguish over the combination of references, and respectfully request reconsideration of the rejection of the claims.

Claim 21

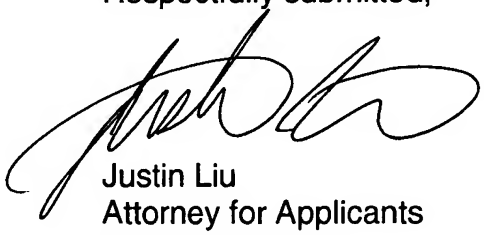
Applicants have similarly amended the method of verifying a semiconductor design of claim 21 to more clearly indicate that the configuration data comprises configuration data for the design of the programmable logic to be tested. Applicants have further amended independent claim 21 to indicate that each system under test of the plurality of systems under test is reconfigured with the design of the programmable logic circuit according to configuration data of the test job by way of the server. Applicants have further amended claim 21 to indicate that corresponding test vectors of the test job for the design of a programmable logic circuit are coupled from a client computer to each system under test by way of the test server. Neither Levi nor Miller discloses or suggests a plurality of client computers coupled to a plurality of systems under test, where the plurality of systems under test are configured with the design of a programmable logic circuit stored in the client computer. Further, neither Levi nor Miller discloses or suggests coupling test vectors of the test job for the design of a programmable logic circuit from the selected client computer to each system under

test by way of the test server. Applicants respectfully request reconsideration of the rejection of independent claim 21 and dependent claims 22-25.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on March 20, 2007

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